AMENDMENTS TO THE CLAIMS

(IN FORMAT COMPLIANT WITH THE REVISED 37 CFR 1.121)

Please cancel claim 17 without prejudice.

1. (CURRENTLY AMENDED) An apparatus comprising:

a full system monitor configured to (i) monitor in real-time ~~(i)~~ one or more software variables down to change rates, (ii) monitor in real-time one or more hardware registers down to cycle rates, ~~and~~ (iii) monitor in real-time one or more firmware registers down to microcode word fetch rates, and (iv) monitor and calculate a frequency of use of each bit in said one or more hardware registers and said one or more firmware registers in response to one or more trigger signals, wherein said one or more trigger signals is generated by a first comparator circuit.

2. (ORIGINAL) The apparatus according to claim 1, wherein said apparatus is configured to monitor said one or more software variables, said hardware registers, and said firmware registers simultaneously.

3. (CURRENTLY AMENDED) The apparatus according to claim 1, wherein said apparatus ~~comprises~~ provides a register level trace.

4. (ORIGINAL) The apparatus according to claim 3, wherein said apparatus is configured to generate one or more log files in response to said monitoring.

5. (ORIGINAL) The apparatus according to claim 1, wherein said apparatus is configured to selectively monitor a specific one or more of said software variables, hardware registers, and firmware registers.

6. (ORIGINAL) The apparatus according to claim 1, wherein said apparatus further comprises software, hardware and firmware register coverage.

7. (ORIGINAL) The apparatus according to claim 1, wherein said apparatus is configured to selectively monitor one or more of said hardware and firmware registers to implement one or more of a verification self-test, a diagnostic method, and monitoring for firmware and software development.

8. (ORIGINAL) The apparatus according to claim 3, wherein said apparatus further comprises one or more user defined start/stop triggers configured to start/stop one or more of said firmware registers, said hardware registers, and said software variables.

9. (ORIGINAL) The apparatus according to claim 1, wherein said monitor is configured to generate a time stamp of a monitor time.

10. (ORIGINAL) The apparatus according to claim 1, wherein said apparatus comprises monitoring hardware configured to connect to one or more internal busses of said system such that the monitoring is non-intrusive.

11. (PREVIOUSLY PRESENTED) The apparatus according to claim 1, wherein said apparatus comprises one or more comparators within said first comparator circuit configured to monitor one or more of an address, data, and a trigger trace.

12. (ORIGINAL) The apparatus according to claim 1, wherein said apparatus is configured to generate a trigger for trace and (i) said trigger is generated in response to one or more of a cycle and a register-delta and (ii) said register-delta comprises a difference between a previous value and a current value registered at one or more of said hardware and firmware registers.

13. (PREVIOUSLY PRESENTED) The apparatus according to claim 12, wherein said apparatus further comprises a CPU configured

to (i) log said trace in response to polling the frequency of a read/write operation of said hardware and firmware register or said trigger signal.

14. (ORIGINAL) The apparatus according to claim 13, wherein said apparatus further comprises a memory configured to log said trace.

15. (ORIGINAL) The apparatus according to claim 9, wherein said apparatus is further configured to generate an analysis of time difference that corresponds to values monitored on said software variables and said hardware and firmware registers.

16. (ORIGINAL) The apparatus according to claim 3, wherein said apparatus is configured to generate post-processing of said trace to assess register coverage.

17. (CANCELED)

18. (ORIGINAL) The apparatus according to claim 10, wherein said monitoring hardware is configured to generate a time stamp of a monitor time.

19. (ORIGINAL) The apparatus according to claim 11, wherein said apparatus is further configured to generate an analysis of filtering trace and capture that corresponds to one or more values monitored on said software variables and said hardware and firmware registers.

20. (ORIGINAL) The apparatus according to claim 11, wherein said apparatus is configured to define one or more windows configured to enable (i) said trace and (ii) a capture.

21. (PREVIOUSLY PRESENTED) The apparatus according to claim 10, wherein said apparatus is configured to filter bit levels of said hardware and firmware registers, such that remaining bits in said full system after said filtering can be assessed to achieve coverage.

22. (ORIGINAL) The apparatus according to claim 1, wherein said apparatus comprises software defined monitor, trace and capture in hardware, software and firmware that correspond to trigger, log depth and trace windows.

23. (ORIGINAL) The apparatus according to claim 9, wherein said apparatus is configured to generate a granularity of

said time stamp between system events and register events that are monitored.

24. (CURRENTLY AMENDED) A method for full system real-time monitoring comprising the steps of:

(A) monitoring one or more software variables down to change rates;

(B) monitoring one or more hardware registers down to cycle rates;

(C) monitoring one or more firmware registers down to microcode word fetch rates;

(D) monitoring a frequency of use of each bit in said one or more hardware registers and said one or more firmware registers;

(E) calculating a frequency of use of each bit in said one or more hardware registers and said one or more firmware registers; and

~~(D)~~(F) generating one or more trigger signals with a first comparator circuit to trigger said full system to monitor in real time.

25. (ORIGINAL) A computer readable medium containing one or more sets of computer executable instructions for performing the steps of claim 24.